**CLAIMS**

1. A system comprising:

a first circuit configured to convert between (i) a serial signal on a first differential interface and (ii) a parallel signal;

a pair of non-crossing conductive paths connecting said first differential interface with a second differential interface; and

a second circuit configured to invert said parallel signal in response to a control signal in an inverting state.

2. The system according to claim 1, wherein inverting said parallel signal is independently inverting each bit of said parallel signal.

3. The system according to claim 1, wherein said second circuit is further configured to buffer said parallel signal in response to said control signal in a non-inverting state.

4. The system according to claim 1, wherein said second circuit comprises:

a plurality of inverters configured to invert each bit of said parallel signal to present an inverted parallel signal; and

a multiplexer configured to select between said parallel signal and said inverted parallel signal in response to said control signal.

5. The system according to claim 1, wherein said second circuit comprises a plurality of exclusive-OR gates each configured to receive (i) one bit of said parallel signal and (ii) said control signal.

6. The system according to claim 1, wherein said second circuit comprises (i) a pass gate and (ii) a tri-state inverter for each bit of said parallel signal.

7. A method of communicating on a differential serial bus, the method comprising the steps of:

(A) converting between a serial signal at a first differential interface and a parallel signal;

(B) routing said differential serial signal between said first differential interface and a second differential interface on non-crossing paths; and

(C) inverting said parallel signal in response to a control signal in an inverting state.

8. The method according to claim 7, wherein said inverting said parallel signal is independently inverting each bit of said parallel signal.

9. The method according to claim 7, further comprising the step of buffering said parallel signal in response to said control signal in a non-inverting state.

10. The method according to claim 7, wherein step (C) comprises the sub-steps of:

inverting said parallel signal to present an inverted parallel signal; and

multiplexing said parallel signal and said inverted parallel signal in response to said control signal.

11. The method according to claim 7, wherein step (C) comprises the sub-step of logically exclusive-OR'ing each bit of said parallel signal with said control signal.

12. The method according to claim 7, wherein step (C) comprises the sub-step of opening a pass gate and activating a tri-state inverter for each bit of said parallel signal in response to said control signal in said inverting state.

13. A system comprising:

means for converting between (i) a serial signal on a first differential interface and (ii) a parallel signal;

a pair of non-crossing conductive paths connecting said first differential interface with a second differential interface; and

means for inverting said parallel signal in response to a control signal in an inverting state.